International **IƆR** Rectifier

IRF7821

HEXFET® Power MOSFET

V_{DSS}	$R_{DS(on)}$ max	Q_g(typ.)
30V	9.1mΩ@V_{GS}= 10V	9.3nC

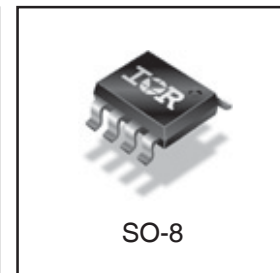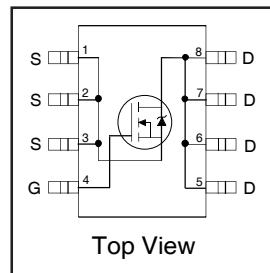## Applications

- High Frequency Point-of-Load Synchronous Buck Converter for Applications in Networking & Computing Systems.

Benefits

- Very Low $R_{DS(on)}$ at 4.5V V_{GS}
- Low Gate Charge
- Fully Characterized Avalanche Voltage and Current

Top View

SO-8

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{DS}	Drain-to-Source Voltage	30	V
V_{GS}	Gate-to-Source Voltage	± 20	
I_D @ T_A = 25°C	Continuous Drain Current, V_{GS} @ 10V	13.6	
I_D @ T_A = 70°C	Continuous Drain Current, V_{GS} @ 10V	11	A
I_{DM}	Pulsed Drain Current ①	100	
P_D @T_A = 25°C	Power Dissipation ④	2.5	W
P_D @T_A = 70°C	Power Dissipation ④	1.6	
	Linear Derating Factor	0.02	W/°C
T_J	Operating Junction and	-55 to + 155	°C
T_{STG}	Storage Temperature Range		

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JL}$	Junction-to-Drain Lead ⑤	——	20	°C/W
$R_{\theta JA}$	Junction-to-Ambient ④⑤	——	50	

Notes ① through ⑤ are on page 10

IRF7821

Static @ T$_J$ = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV$_{DSS}$	Drain-to-Source Breakdown Voltage	30	——	——	V	V$_{GS}$ = 0V, I$_D$ = 250µA
ΔBV$_{DSS}$/ΔT$_J$	Breakdown Voltage Temp. Coefficient	——	0.025	——	V/°C	Reference to 25°C, I$_D$ = 1mA
R$_{DS(on)}$	Static Drain-to-Source On-Resistance	——	7.0	9.1	mΩ	V$_{GS}$ = 10V, I$_D$ = 13A ③
		——	9.5	12.5		V$_{GS}$ = 4.5V, I$_D$ = 10A ③
V$_{GS(th)}$	Gate Threshold Voltage	1.0	——	——	V	V$_{DS}$ = V$_{GS}$, I$_D$ = 250µA
ΔV$_{GS(th)}$	Gate Threshold Voltage Coefficient	——	- 4.9	——	mV/°C	
I$_{DSS}$	Drain-to-Source Leakage Current	——	——	1.0	µA	V$_{DS}$ = 24V, V$_{GS}$ = 0V
		——	——	150		V$_{DS}$ = 24V, V$_{GS}$ = 0V, T$_J$ = 125°C
I$_{GSS}$	Gate-to-Source Forward Leakage	——	——	100	nA	V$_{GS}$ = 20V
	Gate-to-Source Reverse Leakage	——	——	-100		V$_{GS}$ = -20V
gfs	Forward Transconductance	22	——	——	S	V$_{DS}$ = 15V, I$_D$ = 10A
Q$_g$	Total Gate Charge	——	9.3	14		
Q$_{gs1}$	Pre-Vth Gate-to-Source Charge	——	2.5	——		V$_{DS}$ = 15V
Q$_{gs2}$	Post-Vth Gate-to-Source Charge	——	0.8	——	nC	V$_{GS}$ = 4.5V
Q$_{gd}$	Gate-to-Drain Charge	——	2.9	——		I$_D$ = 10A
Q$_{godr}$	Gate Charge Overdrive	——	3.1	——		See Fig. 16
Q$_{sw}$	Switch Charge (Q$_{gs2}$ + Q$_{gd}$)	——	3.7	——		
Q$_{oss}$	Output Charge	——	6.1	——	nC	V$_{DS}$ = 10V, V$_{GS}$ = 0V
t$_{d(on)}$	Turn-On Delay Time	——	6.3	——		V$_{DD}$ = 15V, V$_{GS}$ = 4.5V ③
t$_r$	Rise Time	——	2.7	——		I$_D$ = 10A
t$_{d(off)}$	Turn-Off Delay Time	——	9.7	——	ns	Clamped Inductive Load
t$_f$	Fall Time	——	7.3	——		
C$_{iss}$	Input Capacitance	——	1010	——		V$_{GS}$ = 0V
C$_{oss}$	Output Capacitance	——	360	——	pF	V$_{DS}$ = 15V
C$_{rss}$	Reverse Transfer Capacitance	——	110	——		ƒ = 1.0MHz

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E$_{AS}$	Single Pulse Avalanche Energy ②⑥	——	44	mJ
I$_{AR}$	Avalanche Current ①	——	10	A

Diode Characteristics

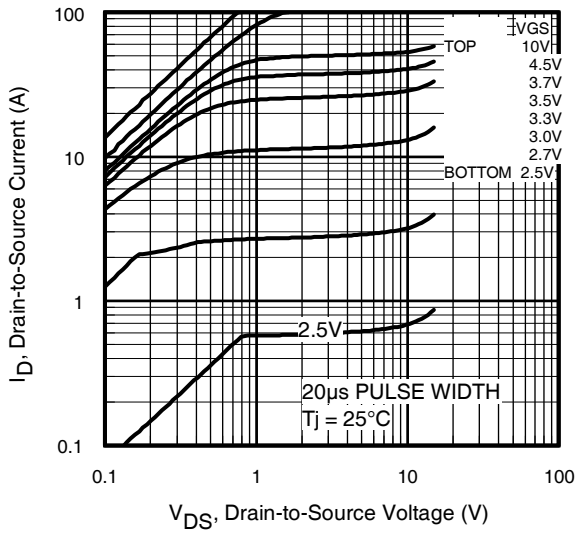|	Parameter	Min.	Typ.	Max.	Units	Conditions
I$_S$	Continuous Source Current (Body Diode)	——	——	3.1	A	MOSFET symbol showing the integral reverse p-n junction diode.
I$_{SM}$	Pulsed Source Current (Body Diode) ①⑥	——	——	100		
V$_{SD}$	Diode Forward Voltage	——	——	1.0	V	T$_J$ = 25°C, I$_S$ = 10A, V$_{GS}$ = 0V ③
t$_{rr}$	Reverse Recovery Time	——	28	42	ns	T$_J$ = 25°C, I$_F$ = 10A, V$_{DD}$ = 20V
Q$_{rr}$	Reverse Recovery Charge	——	23	35	nC	di/dt = 100A/µs ③
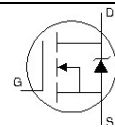
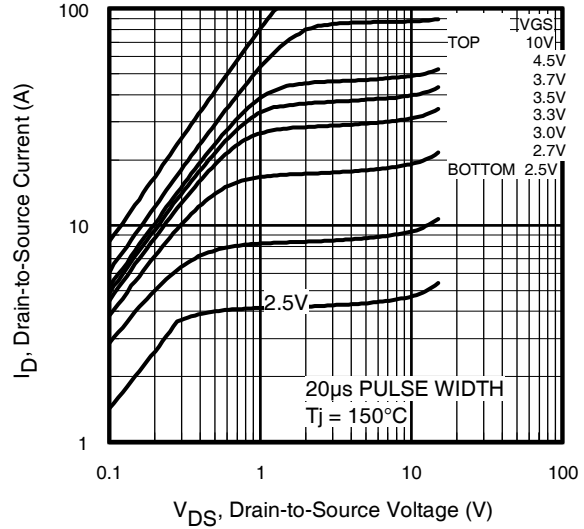**Fig 1.** Typical Output Characteristics
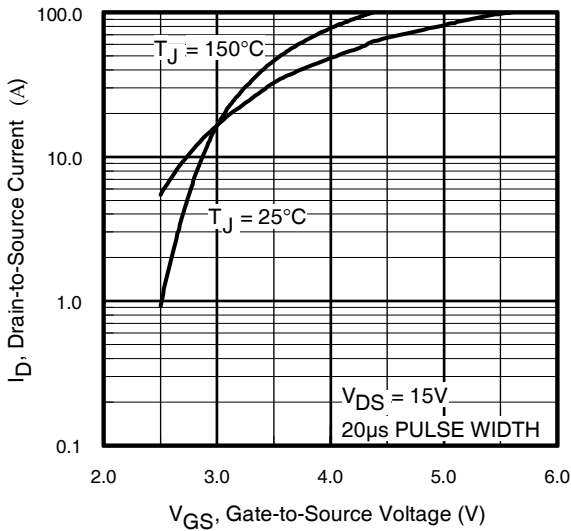
Fig 2. Typical Output Characteristics

Fig 3. Typical Transfer Characteristics
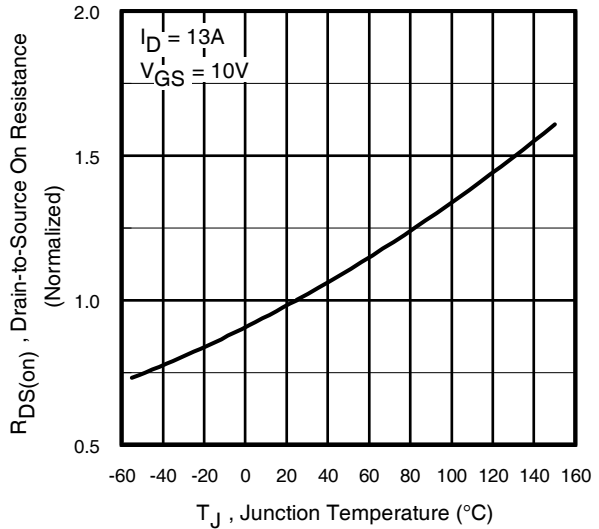
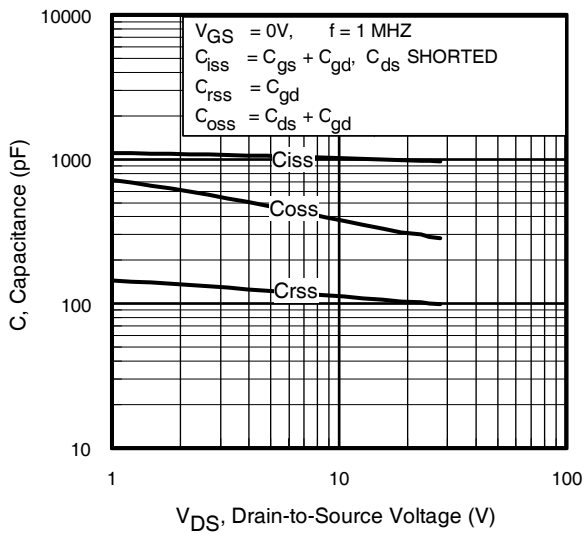**Fig 4.** Normalized On-Resistance Vs. Temperature

IRF7821

International
I⌀R Rectifier

Fig 5 (Typical Capacitance Vs. Drain-to-Source Voltage):

V_{GS} = 0V,   f = 1 MHZ
C_{iss} = C_{gs} + C_{gd}, C_{ds} SHORTED
C_{rss} = C_{gd}
C_{oss} = C_{ds} + C_{gd}

Ciss
Coss
Crss

C, Capacitance (pF)
V_{DS}, Drain-to-Source Voltage (V)

Fig 5. Typical Capacitance Vs.
Drain-to-Source Voltage

Fig 6 (Typical Gate Charge Vs. Gate-to-Source Voltage):

I_D= 10A
V_{DS}= 24V
VDS= 15V

V_{GS}, Gate-to-Source Voltage (V)
Q_G Total Gate Charge (nC)

Fig 6. Typical Gate Charge Vs.
Gate-to-Source Voltage

Fig 7:

T_J = 150°C
T_J = 25°C
V_{GS} = 0V

I_{SD}, Reverse Drain Current (A)
V_{SD}, Source-toDrain Voltage (V)
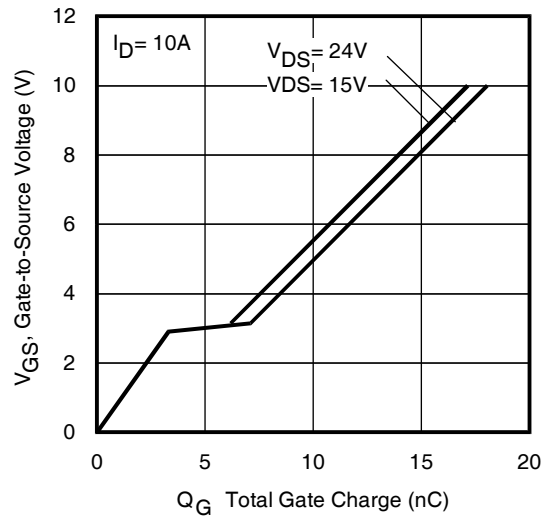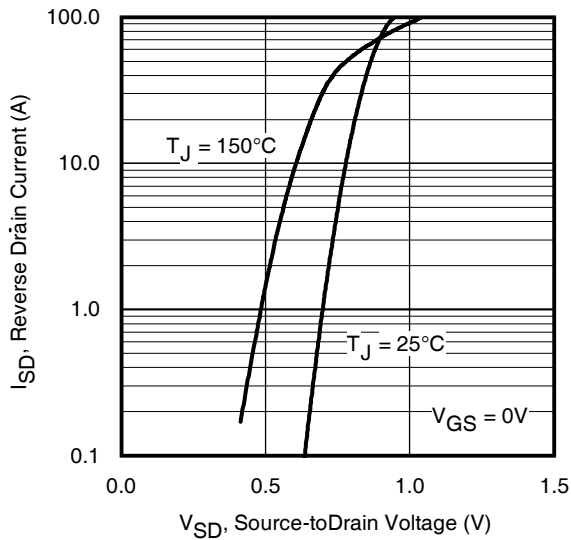
Fig 7. Typical Source-Drain Diode
Forward Voltage

Fig 8:

OPERATION IN THIS AREA
LIMITED BY R_{DS}(on)

100µsec
1msec
10msec

Tc = 25°C
Tj = 150°C
Single Pulse

I_D, Drain-to-Source Current (A)
V_{DS} , Drain-toSource Voltage (V)
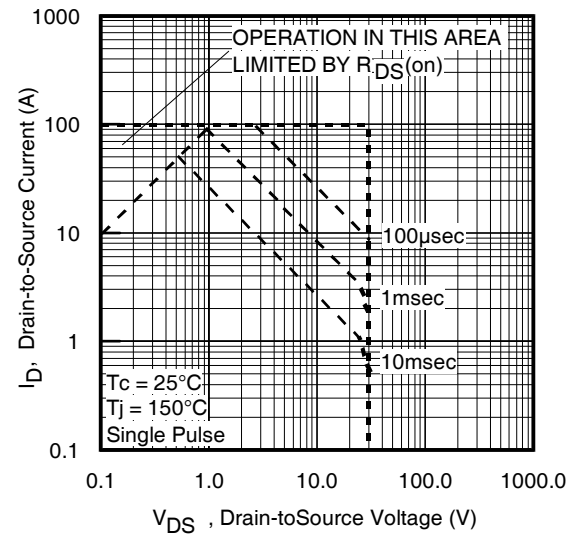
Fig 8. Maximum Safe Operating Area
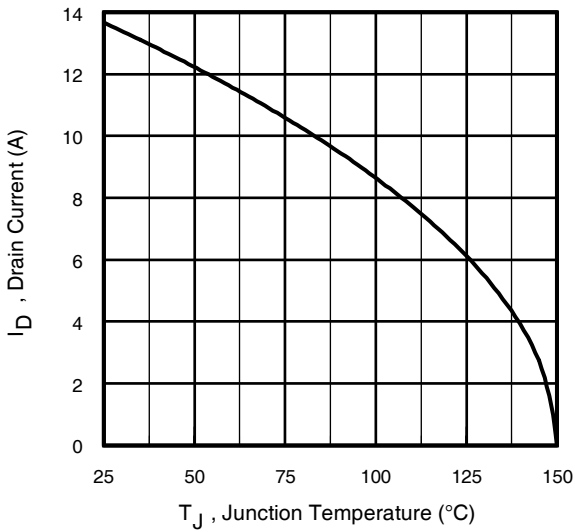
4

IRF7821

Fig 9. Maximum Drain Current Vs. Case Temperature

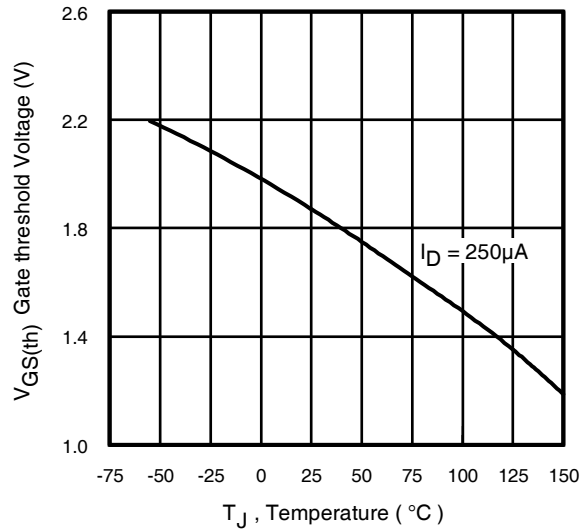**Fig 10.** Threshold Voltage Vs. Temperature
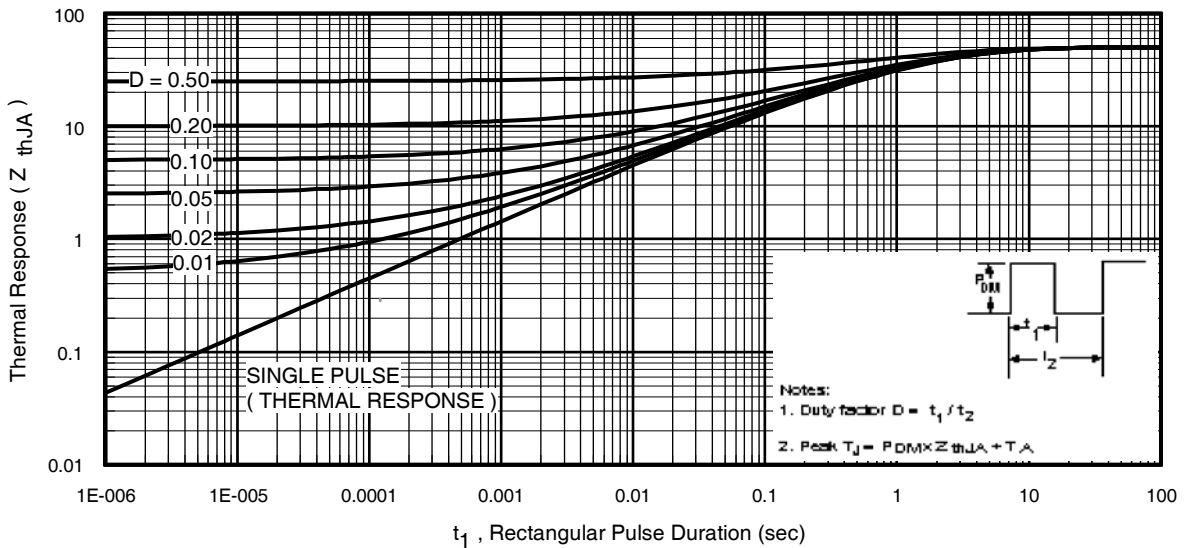

Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

IRF7821

International
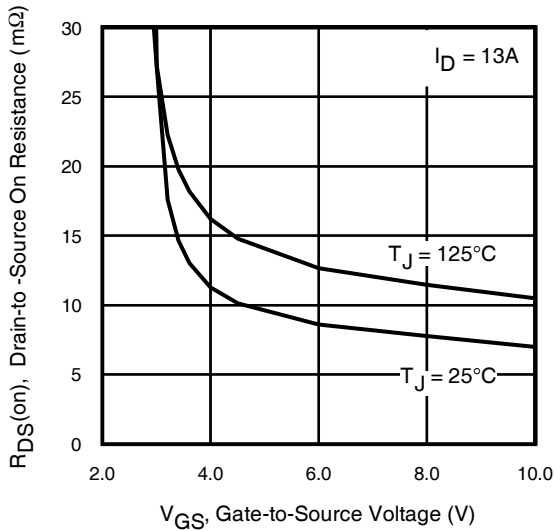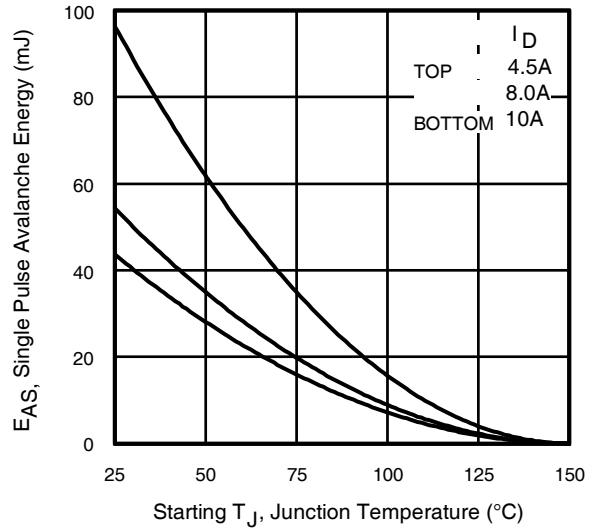**IƆR** Rectifier

Fig 12. On-Resistance Vs. Gate Voltage
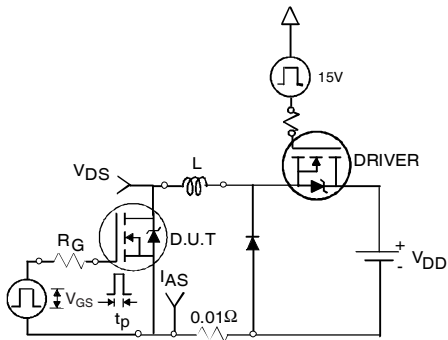

Fig 13c. Maximum Avalanche Energy
Vs. Drain Current
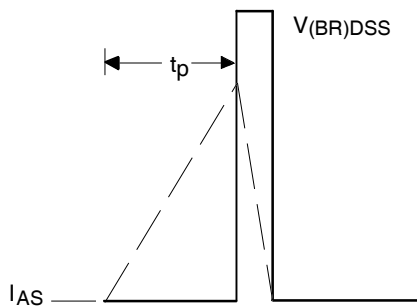

Fig 13a. Unclamped Inductive Test Circuit

Fig 14a. Switching Time Test Circuit

Fig 13b. Unclamped Inductive Waveforms

Fig 14b. Switching Time Waveforms

6

www.irf.com

D.U.T

Circuit Layout Considerations
- Low Stray Inductance
- Ground Plane
- Low Leakage Inductance
  Current Transformer

R_G

- dv/dt controlled by R_G
- Driver same type as D.U.T.
- I_{SD} controlled by Duty Factor "D"
- D.U.T. - Device Under Test

V_{DD}

① Driver Gate Drive

P.W. Period $D = \frac{P.W.}{Period}$

$V_{GS}=10V$*

② D.U.T. I_{SD} Waveform

Reverse Recovery Current

Body Diode Forward Current

di/dt

③ D.U.T. V_{DS} Waveform

Diode Recovery dv/dt

V_{DD}

Re-Applied Voltage

Body Diode Forward Drop

④ Inductor Curent

Ripple ≤ 5%

I_{SD}
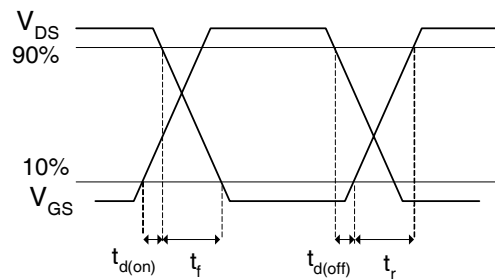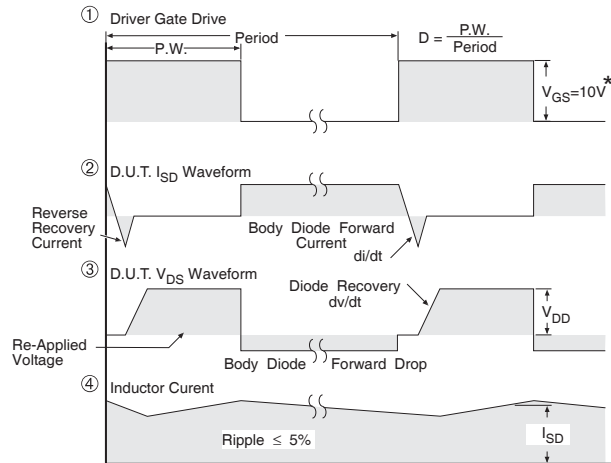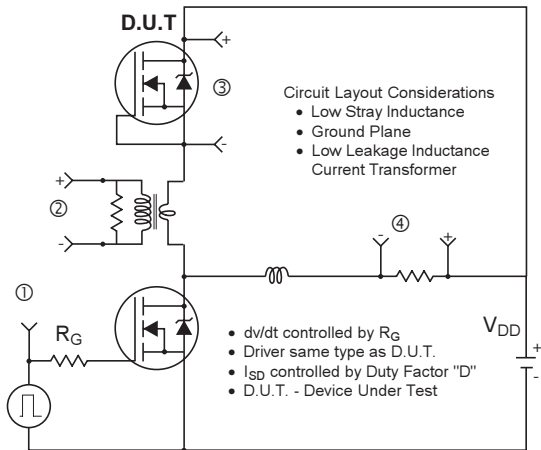
* V_{GS} = 5V for Logic Level Devices

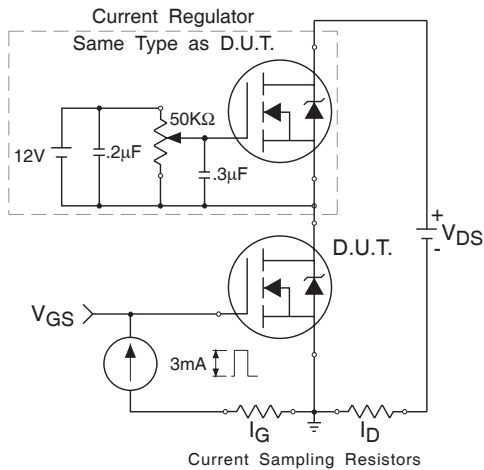**Fig 15.** Peak Diode Recovery dv/dt Test Circuit for N-Channel
HEXFET® Power MOSFETs

Current Regulator
Same Type as D.U.T.

12V .2µF 50KΩ .3µF

V_{DS}

D.U.T.

V_{GS}

3mA

I_G I_D

Current Sampling Resistors

Vds

Id

Vgs

Vgs(th)

Qgs1 Qgs2 Qgd Qgodr

Fig 16. Gate Charge Test Circuit
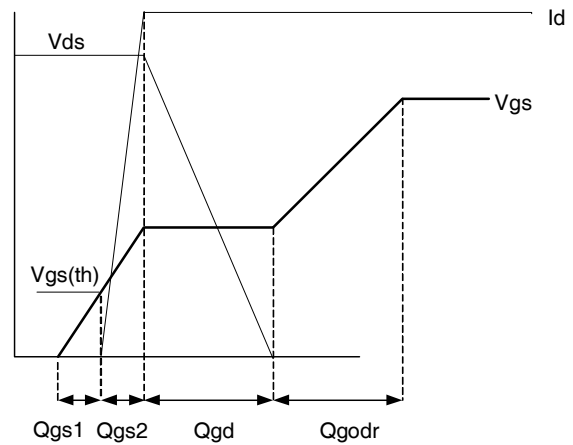
Fig 17. Gate Charge Waveform

IRF7821

Power MOSFET Selection for Non-Isolated DC/DC Converters

Control FET

Special attention has been given to the power losses in the switching elements of the circuit - Q1 and Q2. Power losses in the high side switch Q1, also called the Control FET, are impacted by the $R_{ds(on)}$ of the MOSFET, but these conduction losses are only about one half of the total losses.

Power losses in the control switch Q1 are given by;

$$P_{loss} = P_{conduction} + P_{switching} + P_{drive} + P_{output}$$

This can be expanded and approximated by;

$$P_{loss} = \left(I_{rms}^{2} \times R_{ds(on)} \right)$$
$$+ \left(I \times \frac{Q_{gd}}{i_g} \times V_{in} \times f \right) + \left(I \times \frac{Q_{gs2}}{i_g} \times V_{in} \times f \right)$$
$$+ \left(Q_g \times V_g \times f \right)$$
$$+ \left(\frac{Q_{oss}}{2} \times V_{in} \times f \right)$$

This simplified loss equation includes the terms Q_{gs2} and Q_{oss} which are new to Power MOSFET data sheets.

Q_{gs2} is a sub element of traditional gate-source charge that is included in all MOSFET data sheets. The importance of splitting this gate-source charge into two sub elements, Q_{gs1} and Q_{gs2}, can be seen from Fig 16.

Q_{gs2} indicates the charge that must be supplied by the gate driver between the time that the threshold voltage has been reached and the time the drain current rises to I_{dmax} at which time the drain voltage begins to change. Minimizing Q_{gs2} is a critical factor in reducing switching losses in Q1.

Q_{oss} is the charge that must be supplied to the output capacitance of the MOSFET during every switching cycle. Figure A shows how Q_{oss} is formed by the parallel combination of the voltage dependant (non-linear) capacitance's C_{ds} and C_{dg} when multiplied by the power supply input buss voltage.

Synchronous FET

The power loss equation for Q2 is approximated by;

$$P_{loss} = P_{conduction} + P_{drive} + P_{output}^{*}$$
$$P_{loss} = \left(I_{rms}^{2} \times R_{ds(on)} \right)$$
$$+ \left(Q_g \times V_g \times f \right)$$
$$+ \left(\frac{Q_{oss}}{2} \times V_{in} \times f \right) + \left(Q_{rr} \times V_{in} \times f \right)$$

*dissipated primarily in Q1.

For the synchronous MOSFET Q2, $R_{ds(on)}$ is an important characteristic; however, once again the importance of gate charge must not be overlooked since it impacts three critical areas. Under light load the MOSFET must still be turned on and off by the control IC so the gate drive losses become much more significant. Secondly, the output charge Q_{oss} and reverse recovery charge Q_{rr} both generate losses that are transfered to Q1 and increase the dissipation in that device. Thirdly, gate charge will impact the MOSFETs' susceptibility to Cdv/dt turn on.

The drain of Q2 is connected to the switching node of the converter and therefore sees transitions between ground and V_{in}. As Q1 turns on and off there is a rate of change of drain voltage dV/dt which is capacitively coupled to the gate of Q2 and can induce a voltage spike on the gate that is sufficient to turn the MOSFET on, resulting in shoot-through current . The ratio of Q_{gd}/Q_{gs1} must be minimized to reduce the potential for Cdv/dt turn on.
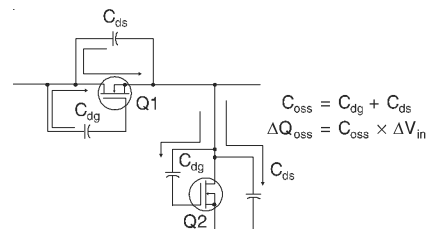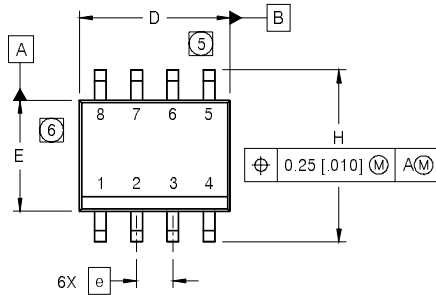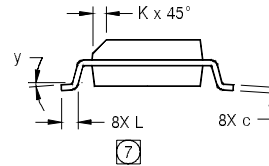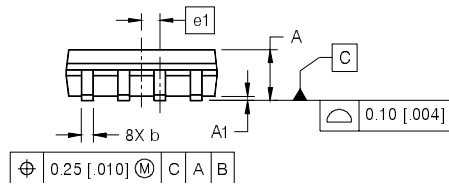

Figure A: Q_{oss} Characteristic

SO-8 Package Details

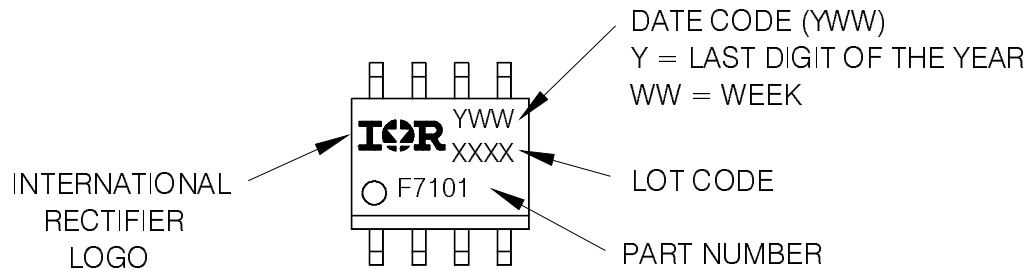| DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e 1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°

NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [.006].
6. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].
7. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.
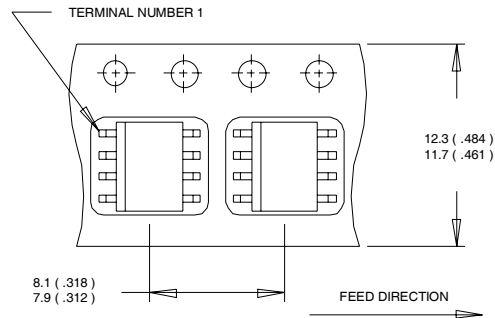
FOOTPRINT
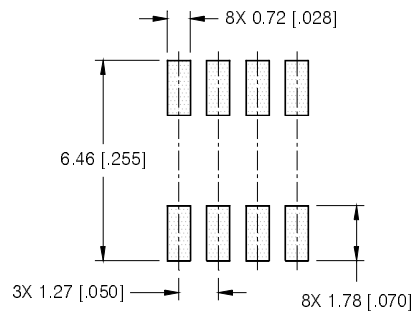
## SO-8 Part Marking

EXAMPLE: THIS IS AN IRF7101 (MOSFET)

DATE CODE (YWW)
Y = LAST DIGIT OF THE YEAR
WW = WEEK

INTERNATIONAL
RECTIFIER
LOGO

LOT CODE

PART NUMBER

International
IƧR Rectifier

SO-8 Tape and Reel

TERMINAL NUMBER 1

12.3 (.484)
11.7 (.461)

8.1 (.318)
7.9 (.312)

FEED DIRECTION

NOTES:
1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS(INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.

∅ 330.00
(12.992)
MAX.

14.40 (.566)
12.40 (.488)
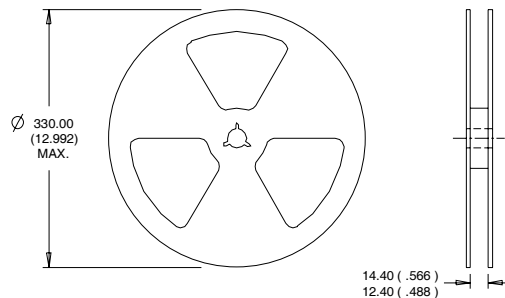
NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Notes:

① Repetitive rating; pulse width limited by
   max. junction temperature.

② Starting T_J = 25°C, L = 0.87mH
   R_G = 25Ω, I_{AS} = 10A.

③ Pulse width ≤ 400μs; duty cycle ≤ 2%.

④ When mounted on 1 inch square copper board

⑤ R_θ is measured at T_J approximately 90°C

Note: For the most current drawing please refer to IR website at http://www.irf.com/package/pkhexfet.html
Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

International
IƧR Rectifier